Two-dimensional Heterojunction Interlayer Tunneling Field Effect Transistors (Thin-TFETs)

Mingda (Oscar) Li, David Esseni, Joseph J. Nahas, Debdeep Jena, and Huili Grace Xing

***Abstract*—The 2D crystals embrace the unique features of the atomically thin bodies, the dangling bond free interfaces, and step-like 2D density of states. To exploit these features for the design of a steep slope transistor, we propose a Two-dimensional Heterojunction Interlayer Tunneling Field Effect Transistor (Thin-TFET) to reach a steep subthreshold swing (SS) of $\sim$14 mV/dec and a high on-current of $\sim$300 μA/μm. The SS is ultimately limited by the density of states broadening at the band edges and the on-current density is estimated on the basis of the interlayer charge transfer time measured in recent experimental studies. A potential material system of monolayer $WSe_2/SnSe_2$ heterojunction can be used to build both n-type and p-type Thin-TFETs. Non-ideality effects such as the non-uniform van der Waals gap thickness between two 2D semiconductors and the finite access resistances are also studied. Finally, the benchmarking for digital applications shows the Thin-TFETs may outperform MOSFETs in term of both performance and energy consumption at low supply voltages..**

***Index Terms*—Tunnel FET, 2D crystals, transport model, benchmarking**

I. Introduction

TUNNEL Field Effect Transistors (FETs) are perceived as promising transistors that may enable scaling supply voltage V_{DD} down to 0.5 V or lower by reducing the subthreshold swing (SS) below 60 mV/dec at room temperature. To date, numerous Tunnel FETs have been demonstrated, among which the heterostructures with near broken gap band alignment are favored in order to achieve sub-60 mV/dec SS and high on currents simultaneously [1]. Tunnel FETs also require a very strong gate control over the channel region to obtain sub-60 mV/dec SS values, which in turn demands ultra-thin body or narrow nanowire structures, where size induced quantization enlarges the bandgap and impedes the realization of near broken gap alignment [2]–[4]. 2D layered crystals, such as monolayers of transition metal dichalcogenides (TMD) MX_2 (e.g. M = Mo, W, Sn; X = S, Se, Te), offer a native thickness of about 0.6 nm with a variety of bandgaps and band-alignments [4], [5], as well as a sharp turn on of density of states at the band edges and the absence of interface dangling bonds, which are highly desired for achieving a sharp SS [6]. Recent experimental results show that the monolayer 2D crystals heterojunction band alignment can be directly controlled by applying perpendicular electric field [7] and the charge transfer in monolayer 2D crystals heterojunction is reasonably fast [8]. In such a contest, a Two-dimensional Heterojunction Interlayer Tunneling FET (Thin-TFET) based on a vertical arrangement of 2D layered materials is proposed. In particular, we discuss both n-type and p-type Thin-TFETs employing the potential material system of 2H-WSe_2 and 1T-$SnSe_2$. Our simulations suggest that the Thin-TFETs can achieve very competitive SS values and a high on-current. Along with the low gate-to-drain and gate-to-source capacitance, the Thin-TFETs enable fast switching and low energy consumption. The effect of non-uniform van der Waals gap thickness and the external source and drain total access resistance are also discussed. Experimental efforts have been carried out to demonstrate the Thin-TFET based on $WSe_2/SnSe_2$ heterojunction. Some experimental insights are shared at the end of the paper.

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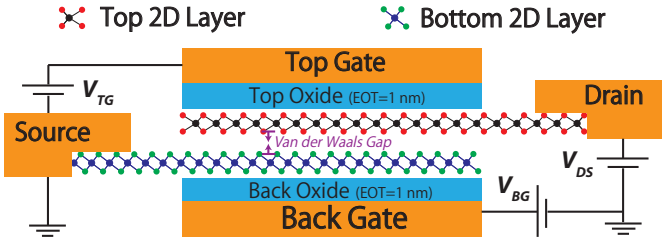

Fig. 1. The schematic device layer structure of the Thin-TFET

II. Device Structure and Modeling Approach

The Thin-TFET device structure is shown in Fig.1, where the bottom and top 2D semiconductors act as the source and the drain respectively. The van der Waals gap separates top and bottom 2D semiconductors and the thickness of the van der Waals gap is defined as the distance from the center of the chalcogenide atom in the top 2D layer to the center of the nearest chalcogenide atom in the bottom 2D layer (see Fig.1). The device working principle can be explained as follows: take the p-type Thin-TFET as the example, when E_{CB} is higher than E_{VT} (see Fig.2), tunneling from the bottom layer is inhibited and the device is nominally off. When a negative top gate voltage pulls E_{VT} above E_{CB} (see Fig.3[a]), a tunneling window is opened and a current can flow.

To calculate the band alignment between E_{CB} and E_{VT} along the direction perpendicular to the 2D semiconductors we first use Gauss's law and write [9]

$$\begin{aligned} C_{TOX}V_{TOX} - C_{vdW}V_{vdW} &= e(p_T - n_T + N_T) \\ C_{BOX}V_{BOX} + C_{vdW}V_{vdW} &= e(p_B - n_B + N_B) \end{aligned} \quad (1)$$

where e is the magnitude of electron charge, $C_{T(B)OX}$ is the capacitance per unit area of top (back) oxide, and C_{vdW}

is the capacitance per unit area of the van der Waals gap. $V_{T(B)OX}$ and V_{vdW} are the corresponding potential drops. $n(p)_{T(B)}$ is the electron (hole) densities in the top (bottom) 2D semiconductor layer, and N_T, N_B are the net chemical doping concentrations (donor minus acceptor) in the layers, which are set to zero in this work. The potential drops can be written in terms of the top gate V_{TG}, back gate V_{BG}, and drain-source voltage V_{DS} (which sets the split of the quasi-Fermi levels in the top and bottom semiconductor layers), and of the material properties as

$$\begin{aligned} eV_{vdW} &= eV_{DS} - e\phi_{p,B} - e\phi_{n,T} + E_{GB} + \chi_{2D,B} - \chi_{2D,T} \\ eV_{TOX} &= eV_{TG} + e\phi_{n,T} - eV_{DS} + \chi_{2D,T} - e\Phi_{M,T} \\ eV_{BOX} &= eV_{BG} - e\phi_{p,B} + E_{GB} + \chi_{2D,B} + e\Phi_{M,B} \end{aligned} \tag{2}$$

where we define $e\phi_{n,T(B)}{=}E_{CT(B)}{-}E_{FT(B)}$ and $e\phi_{p,T(B)}{=}E_{FT(B)}{-}E_{VT(B)}$, E_{GB} is the energy gap in the bottom 2D semiconductor and $V_{T(B)OX}$ is the potential drop across the top (back) gate dielectric, V_{vdW} is the potential drop across the van der Waas gap, $\chi_{2D,T(B)}$ is the electron affinity of the top (bottom) 2D semiconductor, and $\Phi_{M,T(B)}$ is the metal workfunction of the top (back) gate (see Fig.2).

By using effective mass approximation and assuming that the majority carriers of the two 2D semiconductors are at thermodynamic equilibrium with their Fermi levels [10], the carrier densities can be written as

$$n(p) = \frac{g_v m_c^*(m_v^*) k_B T}{\pi\hbar^2} \ln\left[\exp\left(-\frac{q\phi_{n,T}(\phi_{p,B})}{k_B T}\right) + 1\right] \tag{3}$$

where g_v is the valley degeneracy and $m_c^*(m_v^*)$ is the conduction (valence) band effective mass.

By inserting Eqs.2 and 3 in Eq.1 we obtain two equations determining $\phi_{n,T}$, $\phi_{p,T}$ and thus the band alignment.

We calculate the tunneling current by using the transfer-Hamiltonian method [11], as recently revisited for resonant tunneling graphene transistors [12], [13]. We here summarize the basic equations; a more thorough discussion can be found in [9]. The tunneling current density, J_T, is expressed as [9]:

$$\begin{aligned} J_T = &\frac{g_v e\,|M_{B0}|^2\,A}{4\pi^3\hbar} \mathrm{e}^{-2\kappa T_{vdW}} \times \\ &\int_{\mathbf{k}_T}\int_{\mathbf{k}_B} d\mathbf{k}_T\, d\mathbf{k}_B\, S_F(q)\, S_E(E_B - E_T)\,(f_B - f_T) \end{aligned} \tag{4}$$

where κ is the decay constant of the wave-function in the van der Waals gap [12], [13], T_{vdW} is the thickness of the van der Waals gap, $\mathbf{k}_{T(B)}$, $E_{T(B)}$ and $f_{T(B)}$ are the wave-vector, the energy and Fermi occupation function in the top (bottom) 2D semiconductor and M_{B0} is the tunneling matrix element [9], which is a property of the material system and is further discussed in Sec.III. Eq.4 assumes that in the tunneling process electrons interact with a random scattering potential, whose spectrum is taken as $S_F(q){=}\,\pi L_C^2/(1+\mathbf{q}^2L_C^2/2)^{3/2}$, where $q{=}|\mathbf{k}_T{-}\mathbf{k}_B|$ and L_C is the correlation length. The scattering relaxes the momentum conservation, i.e. allowing tunneling for $\mathbf{k}_B{\neq}\mathbf{k}_T$. A similar $S_F(q)$ has been used to analyze the resonance linewidth in graphene tunneling transistors [13]. The $S_F(\mathrm{q})$ may be representative of different scattering mechanisms that are discussed in [9], [13]. Finally $S_E(E){=}\exp(-E^2/\sigma^2)/(\sqrt{\pi}\sigma^2)$ describes the energy broadening in the 2D semiconductors, where σ is the energy broadening parameter [9]. The contact resistance is included by self-consistently calculating the tunnel current density and the voltage drop on the total access resistance in our model.

III. Simulation Results and Discussions

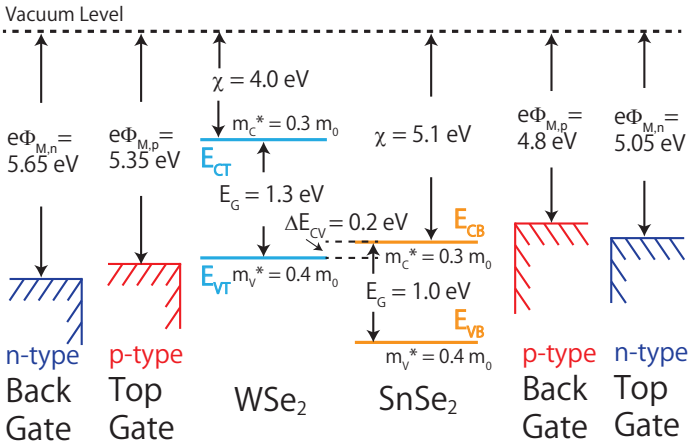

Fig. 2. For the n-type Thin-TFET, $SnSe_2$ is the top 2D layer and WSe_2 is the bottom 2D layer, along with the top and back gate labeled as n-type in blue. While for the p-type Thin-TFET, WSe_2 is the top 2D layer and $SnSe_2$ is the bottom 2D layer, along with the top and back gate labeled as p-type in red; Band gaps, electron affinities, effective masses are shown for WSe_2 and $SnSe_2$. The n-type and p-type metal work functions are tuned to give symmetric threshold voltages for the n-type and p-type Thin-TFETs.

A. Material system and n-type & p-type Thin-TFETs

$C_{G,avg}$ Out of various 2D semiconductors studied by density function theory calculations [5] and various experimental efforts, we chose the trigonal prismatic coordination monolayer WSe_2 and the octahedral coordination (CdI_2 crystal structure) monolayer $SnSe_2$ (see Fig.2). Since there is no experimental band structure reported for *monolayer* WSe_2 and $SnSe_2$, the potential band alignment of the $WSe_2/SnSe_2$ system used in this work are based on the existing experimental results of *multilayer* WSe_2 and $SnSe_2$ [14]–[16] and their approximated effective masses are based on the DFT results [5] (see Fig.2). $WSe_2/SnSe_2$ heterojunction can potentially form a staggered or near broken band alignment, which reduces the voltage drop in the van der Waals gap in the on-state condition [1] and also help to suppress the thermionic leakage current. Also, $SnSe_2$ tends to be an n-type semiconductor [17], [18] and WSe_2 can be electrostatically doped to be p-type [19]. Therefore, if one considers the p-type Thin-TFET as an example, by applying negative top gate voltage V_{TG}, the top layer WSe_2 can be electrostatically tuned to be more p-type (see Fig.3[e]) in order to open the tunnel window, while the bottom layer $SnSe_2$ stays n-type (see Fig.3[e]) and screens most electrical field from the top layer so as to maximize the potential drop across the $WSe_2/SnSe_2$ heterojunction induced by the gate voltage. It is also worth noting that there may be dipoles on the $WSe_2/SnSe_2$ interface [15], so that the electron

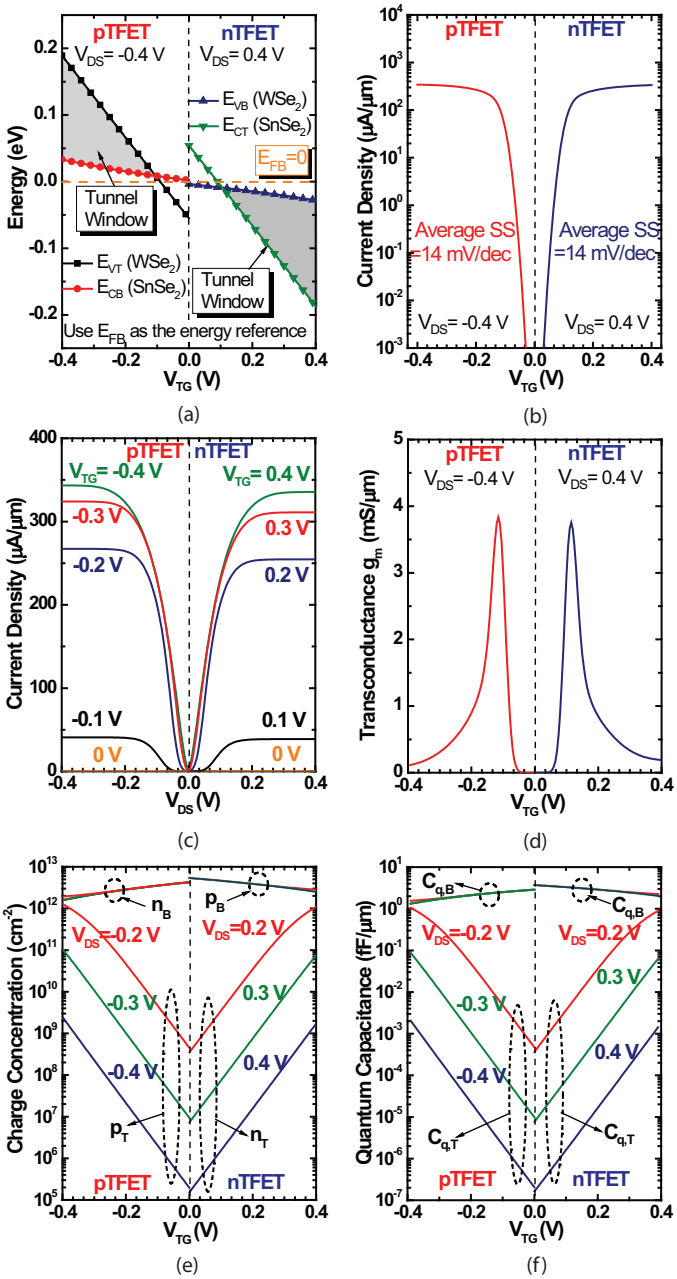

Fig. 3. For both the n-type Thin-TFET and the p-type Thin-TFET (a) the band alignment versus V_{TG}; (b) Current density versus V_{TG}, the average SS is calculated from 10^{-3} μA/μm to 10 μA/μm; (c) the current density versus V_{DS} at various V_{TG}; (d) the transconductance versus V_{TG}; (e) the carrier concentration in the top and bottom 2D layers versus V_{TG} at various V_{DS}; (f) the quantum capacitances of the top and bottom 2D layers versus V_{TG} at various V_{DS};

affinity rule requires some modifications, although interfacial dipoles are not considered in this work.

Following the complex band method [20], we assume the effective barrier height E_B of the van der Waals gap is 1 eV and the electron mass in the van der Waals gap is the free electron mass m_0, thus the decay constant is $\kappa = \sqrt{2m_0E_B/\hbar}$ = 5.12 nm^{-1}. In the model, the scattering correlation length L_C in S_F(q) was set to L_C=10 nm, which is also consistent with the value employed in [13]; the energy broadening σ is set to 10 meV. M_{B0} in Eq.4 is directly related to the interlayer charge transfer time $\tau_{b(t)}$ across the van der Waals gap of the carrier in bottom (top) 2D semiconductor, which can be written as [21]

$$\tau_{b(t)}^{-1} = \frac{2\pi}{\hbar}\rho_{t(b)}|M_{B0}|^2 e^{-2\kappa T_{vdW}} S_F(q) \quad (5)$$

where $\rho_{t(b)}(E)$ is the density of states (DOS) of the top (bottom) 2D semiconductors and $\rho_{t(b)}$=g$_v$m$^*_{t(b)}/\pi\hbar^2$. For the n-type Thin-TFET, $\rho_{t(b)}(E)$ is the DOS of the conduction (valence) band of the top (bottom) 2D semiconductor, while for the p-type Thin-TFET, $\rho_{t(b)}(E)$ is the DOS of the valence (conduction) band of the top (bottom) 2D semiconductor. As can be seen from Eq.5 and then the S_F(q) expression (given after Eq.4), due the scattering in our model the τ increases with q, which is the magnitude of the wave-vector difference across the van der Waals gap defined as q=$|\mathbf{k}_T - \mathbf{k}_B|$. Recent experimental results [8] observed the charge transfer time across van der Waals gap between MoS_2 and WS_2 is ~25 fs, which, according to Eq.5, gives us the M_{B0} ~ 0.02 eV when q=0. We recognize that the charge transfer time might be different for different 2D heterojunctions, but it might be reasonable to assume they have similar values. Thus, we choose M_{B0}=0.02 eV in all following simulations.

In all current calculations the top and back oxide have an effective oxide thickness (EOT) of 1 nm, which give the top and back oxide capacitance C_{TG} and C_{BG} of 0.518 fF/μm. The thickness of the van der Waals gap is set to be 3.5 Å, unless specified otherwise. We assume the relative dielectric constant of the van der Waals gap is 1.0 therefore the van der Waals gap capacitance C_{vdW} is 0.38 fF/μm. Throughout this work, the gate length is 15 nm as well as the back gate and the source are grounded. The external total access resistances are neglected unless specified.

The material systems for both the p-type and the n-type Thin-TFET are shown in Fig.2. The n-type and p-type metal work functions are tuned to give symmetric threshold voltages for the n-type and the p-type Thin-TFET. Figure 3[a] shows the band alignment versus V_{TG} curves. As can be seen, the V_{TG} can effectively control the vertical band alignment in the device and, for the p-type Thin-TFET in particular, induce the crossing between E_{VT} and E_{CB}, with E_{CB} being relatively insensitive to V_{TG} compared to E_{VT}. Figure.3[b] shows I_D versus V_{TG} with very compelling average SS (from 10^{-3} μA/μm to 10 μA/μm) of ~14 mV/dec. The I_D versus V_{DS} family curves are shown in Fig.3[c]. I_D is well saturated with V_{DS} when V_{DS}>~0.2 V. The superlinear onset is also observed and the so called V_{DS} threshold voltage increases at lower V_{TG} [22]. The peak transconductances around 4 mS/μm are shown in Fig.3[d], which are much larger than reported peak transconductances of sub-22 nm MOSFET [23], [24]. In Fig.3[e], the top gate changes the carrier concentrations of the top 2D semiconductor much faster than of the bottom 2D semiconductor under different V_{DS}. The ability to efficiently change the hole (electron) concentration in the top 2D semiconductor while keeping the high electron (hole) concentration in the bottom 2D semiconductor is vital to achieve good electrostatics control of the p-type (n-type) Thin-TFET. The values of the so called quantum capacitances are written as

Eq.6:

$$C_{Q,T(B)} = -\left[\frac{e\partial p_{T(B)}}{\partial \phi_{p,T(B)}} + \frac{e\partial n_{T(B)}}{\partial \phi_{n,T(B)}})\right] \quad (6)$$

Figure.3[f] illustrates the quantum capacitances under different bias conditions.

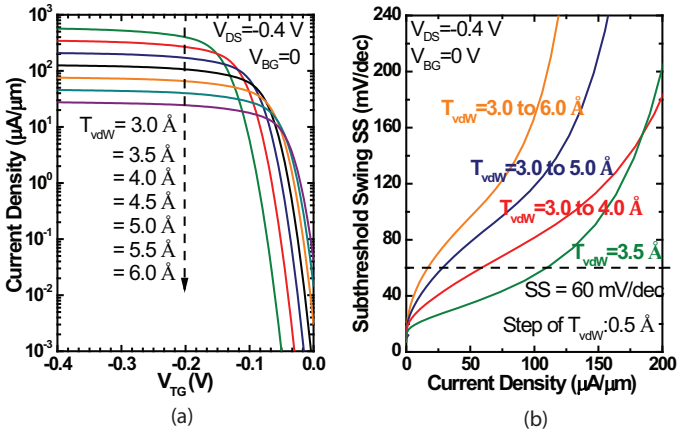

Fig. 4. For the p-type Thin-TFET: (a) tunnel current density versus V_{TG} for different van der Waals gap thicknesses T_{vdW}; (b) SS versus V_{TG} when having equally distributed van der Waals gap thickness T_{vdW} variations;

B. Effects of non-uniform van der Waals gap thicknesses and Total Access Resistances

Due to the nature of van der Waals bonds, the van der Waals gap thickness is subject the interlayer rotational alignment of the two 2D semiconductors [25]. Meanwhile, the tunneling probability is very sensitive to the tunneling distance, namely the van der Waals gap thickness, to investigate the effects of non uniform van der Waals thickness. In the instance of p-type Thin-TFET, we vary the van der Waals gap thickness T_{vdW} from 3.0 Å to 6.0 Å with the step of 0.5 Å. As shown in Fig.4[a], the on-current density decreases and the threshold voltage moves towards 0 when increasing the T_{vdW}. The impact on the sub-threshold swing is instead modest whenT_{vdW} is still considered uniform. However, in Fig.4[b], we consider various T_{vdW} values across a heterojunction by assuming the T_{vdW} are equally distributed. For example, for a 2D heterojunction with equally distributed T_{vdW} from 3.0 Å to 5.0 Å with the step of 0.5 Å, we take the I_D-V_{TG} curves for each T_{vdW} (i.e. 3.0 Å, 3.5 Å, 4.0 Å, 4.5 Å, and 5.0 Å) shown in Fig.4[a] and average them to obtain the overall I_D-V_{TG} curve. The SS of the average I_D-V_{TG} curves versus I_D are plotted in Fig.5[b] with difference T_{vdW} variation ranges. For the van der Waals gap with equally distributed deviations, the SS increases with increasing variation ranges. For a randomly distributed van der Waals gap thicknesses, this trend is also expected.

Since the total access resistances have become critical to ultra-scaled transistors and how to optimize the total access resistance on 2D crystals still remains as an open question, we included the total access resistance R_C in I-V curves calculations. Figure 5[a] shows the I_D versus V_{TG} at V_{DS}=-0.4 V with different R_C: the current density remains almost the same with R_C up to 320 $\Omega\mu$m and decreases with increasing

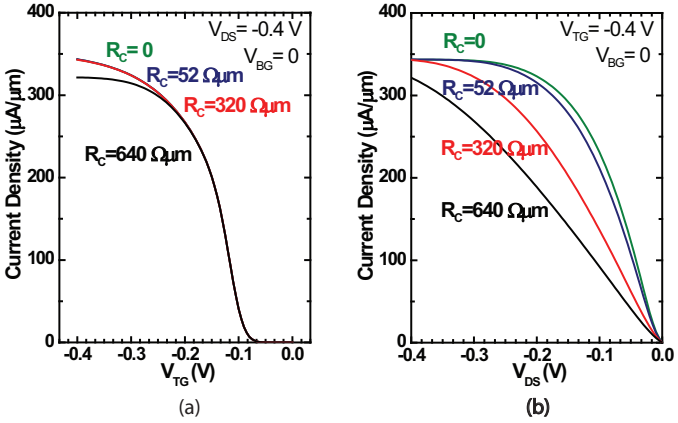

Fig. 5. For the p-type Thin-TFET: (a) the tunnel current density versus V_{DS} at different V_{TG} with total access resistances R_C; (b) the tunnel current density versus V_{DS} with different total access resistances R_C.

R_C. From Fig.5[b], the saturation region of I_D versus V_{DS} curve can be affected when $|V_{DS}|$<0.4 V if $R_C > \sim$52 $\Omega\mu$m. In an ideal 2D conductor, the total access resistance is around $\sim$52 $\Omega\mu$m for a degenerate 2D semiconductor and is around $\sim$325 $\Omega\mu$m for an nondegenerate 2D semiconductor [26]. Thus the access region of 2D semiconductors must be degenerately doped to approach the optimal R_C.

C. Capacitance Evaluation

The gate-to-drain and gate-to-source capacitances (i.e. C_{GD}, C_{GS}) can be readily calculated from the capacitance network shown in Fig.6. The quantum capacitances $C_{Q,T(B)}$ of the top

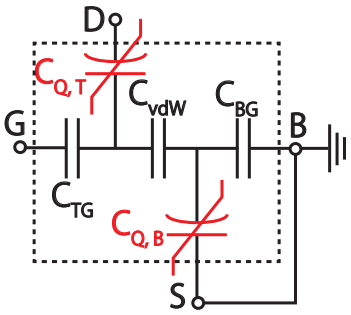

Fig. 6. Capacitance network model of the Thin-TFET

(bottom) 2D semiconductor are defined in Eq.6 and indicated as the red non-linear capacitances in Fig.6. First we define C_S and C_T as:

$$\begin{aligned} 1/C_S &\equiv 1/C_{vdW} + 1/(C_{Q,B} + C_{BG}) \\ C_T &\equiv C_{TG} + C_{Q,T} + C_S \end{aligned} \quad (7)$$

Then, C_{GD} and C_{GS} can be written as Eqs.8:

$$\begin{aligned} C_{GS} &= \frac{C_{TG}C_S}{C_T} \\ C_{GD} &= \frac{C_{TG}C_{Q,T}}{C_T} \end{aligned} \quad (8)$$

For the p-type Thin-TFET, the source is the bottom 2D semiconductor $SnSe_2$ while the drain is the top 2D semiconductor layer WSe_2 (see Fig.2). The capacitances calculated for the p-type Thin-TFET are shown in Fig.7. From Fig.7[a], C_{GD} is

only significant when the p-type Thin-TFET is in the linear region of the I_D-V_{DS} curve, where the drain is coupled with the top gate to change the tunnel current. While $|V_{DS}|$ further increases, the Thin-TFET enters the saturation region, where the C_{GD} becomes close to zero. On the other hand, C_{GS} remains significantly larger than C_{GD} in the saturation region, indicating the top gate and the source stay closely coupled as desired. But C_{GS} becomes smaller when entering linear region. From Fig.7[b], C_{GD} dramatically increases while C_{GS} decreases when $|V_{TG}|>|V_{DS}|$. In practice, when designing the Thin-TFET as a switch in a digital circuit, we should avoid to bias $|V_{TG}|>|V_{DS}|$ because of losing gate control. The capacitance model will be useful for implementing the Thin-TFET into circuit simulations.

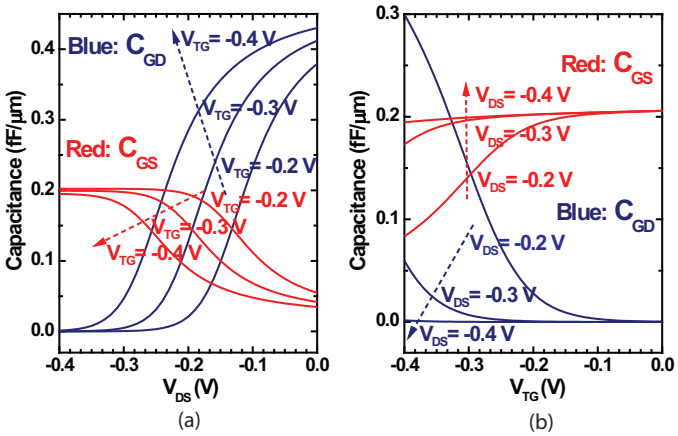

Fig. 7. For the p-type Thin-TFET, (a) C_{GD} and C_{GS} versus V_{DS} at V_{TG}=-0.2, -0.3, -0.4 V; (b) C_{GD} and C_{GS} versus V_{TG} at V_{DS}=-0.2, -0.3, -0.4 V.

D. Benchmarking

The Semiconductor Research Corporation (SRC) Nanoelectronic Research Initiative (NRI) has supported research on beyond CMOS devices as reported by Bernstein, et al. [27] As part of the initiative, a comparison of the projected performance of new devices with the projected performance of CMOS of the same generation (benchmarking) was performed. The benchmarking of beyond CMOS devices in SRC has continued and been standardized by Nikonov and Young [28] [29]. The Thin-TFET research, since it is partially supported by SRC under STARnet, participates in benchmarking using the Nikonov and Young (N&Y) methodology.

The N&Y methodology uses basic device performance parameters such as operating voltage (V_{DD} = $|V_{DS}|$), saturation current (I_{Dsat}), and average gate capacitance ($C_{G,avg}$), to project logic switching energy and switching delay. The change of the net charge under the gate (ΔQ) when V_{TG} switching from 0 to V_{DD} is the sum of the change of the net charge in the top 2D semiconductor and the bottom 2D semiconductor. The average gate capacitance ($C_{G,avg}$) is defined as $\Delta Q/V_{DD}$. Here we take the p-type Thin-TFET as an example, I_{Dsat} and $C_{G,avg}$ are provided in Tab.I for the supply voltages V_{DD} equal to 0.2, 0.3, and 0.4 V and total access resistances R_C equal to 52 and 320 $\Omega\mu$m, projected values for intrinsic switching energies and intrinsic switching delays are generated using the N&Y methodology and are plotted as shown in Fig. 8. The device parameters for High Performance (HP) CMOS and Low Power (LP) CMOS are taken from Ref. [29] and we use the same geometrical parameters for both the CMOS and Thin-TFET are shown in Tab.I. Also, we ignore the contact capacitance [29] in this benchmarking.

TABLE I
BENCHMARKING PARAMETERS FOR THIN-TFETS WITH DIFFERENT V_{DD} AND R_C, DEVICE PARAMETERS FOR HP CMOS AND LP CMOS, AND GEOMETRICAL PARAMETERS FOR BOTH THE CMOS AND THE THIN-TFET

Parameters for Thin-TFETs with Different V_{DD} and R_C						
V_{DD} (V)	**0.2**		**0.3**		**0.4**	
R_C ($\Omega\mu$m)	**52**	**320**	**52**	**320**	**52**	**320**
I_{Dsat} (μA/μm)	263	233	325	317	349	348
ΔQ (mC/m^{-2})	2.34	2.80	3.33	3.72	4.30	4.47
$C_{G,avg}$ (fF/μm)	0.175	0.210	0.167	0.186	0.161	0.168
Parameters for HP and LP CMOS [29]						
	V_{DD} (V)		**I_{Dsat} (μA/μm)**		**C_G (fF/μm)**	
HP CMOS	0.73		1805		1.29	
LP CMOS	0.3		2		1.29	
Geometrical Parameters for Benchmarking						
Half-pitch (nm)	EOT (nm)		Gate Length (nm)		Gate Width (nm)	
15	1		15		60	

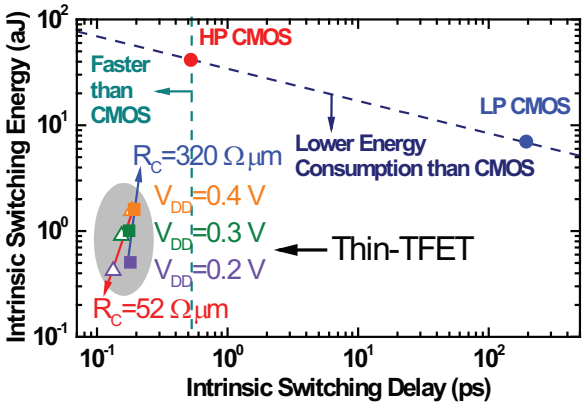

Fig. 8. The intrinsic switching energy and intrinsic switching delay for HP CMOS, LP CMOS, and Thin-TFET with V_{DD}=0.2, 0.3, 0.4 V and R_C=52, 320 $\Omega\mu$m.

Note that the Thin-TFET is projected to be able to operate down to a supply voltage of 0.2 V which provides a distinct energy consumption and performance advantage.

E. Experimental Insights

While trying to demonstrate Thin-TFET experimentally, some key challenges have been identified. First, the current Dry Transfer is not suitable for integrated circuit processes [30]. The Molecular Beam Epitaxy 2D crystal heterojunctions have been grown but the grain size is in the order of several nanometers [31]. Second, efficient top gate control requires a high quality and interfacial state free dielectrics. Atomic layer deposition has been improved over years to achieve good quality gate dielectrics on 2D crystals [32]. Using 2D dielectrics such as hexagonal boron nitride as the gate dielectrics has also been pursued [33]. Third, low resistance ohmic contacts to 2D crystal are vital to device performance.

Various techniques such as external chemical doping [34], internal chemical doping [35], electrostatic doping such as ion doping [36] and phase-engineering from the semiconductor phase to the metallic phase of a 2D crystal [37], have been implemented to reduce the contact resistances. Last but not least, with the material properties remain unclear for most 2D crystals, a lot of initial effort will be put into understanding the materials characteristics.

IV. Conclusion

A new tunnel transistor, Thin-TFET, has been proposed and possible material systems are identified. Simulations based on the transfer Hamiltonian method suggest that the Thin-TFETs can achieve very good sub-threshold swing (SS) and high on-current, and are thus promising devices for ultra-low energy digital systems.

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References

[1] G. Zhou, R. Li, T. Vasen, M. Qi, S. Chae, Y. Lu, Q. Zhang, H. Zhu, J.-M. Kuo, T. Kosel *et al.*, "Novel gate-recessed vertical InAs/GaSb TFETs with record high I_{ON} of 180 μA/μm at V_{DS}= 0.5 V," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, pp. 32–6.

[2] S.Brocard, M.Pala, and D.Esseni, "Design options for hetero-junction tunnel FETs with high on current and steep sub-V_T slope," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012, p. 5.4.1.

[3] Y. Lu, G. Zhou, R. Li, Q. Liu, Q. Zhang, T. Vasen, S. Doo Chae, T. Kosel, M. Wistey, H. Xing, A. Seabaugh, and P. Fay, "Performance of AlGaSb/InAs TFETs with gate electric field and tunneling direction aligned," *Electron Device Letters, IEEE*, vol. 33, no. 5, pp. 655–657, May 2012.

[4] D. Jena, "Tunneling transistors based on graphene and 2-d crystals," *Proceedings of the IEEE*, vol. 101, no. 7, pp. 1585–1602, July 2013.

[5] C. Gong, H. Zhang, W. Wang, L. Colombo, R. M. Wallace, and K. Cho, "Band alignment of two-dimensional transition metal dichalcogenides: Application in tunnel field effect transistors," *Applied Physics Letters*, vol. 103, no. 5, pp. 053 513–053 513, 2013.

[6] S. Agarwal and E. Yablonovitch, "Using dimensionality to achieve a sharp tunneling FET (TFET) turn-on," in *Device Research Conference (DRC), 2011 69th Annual*. IEEE, 2011, pp. 199–200.

[7] P. Rivera, J. R. Schaibley, A. M. Jones, J. S. Ross, S. Wu, G. Aivazian, P. Klement, N. J. Ghimire, J. Yan, D. Mandrus *et al.*, "Observation of long-lived interlayer excitons in monolayer mose2-wse2 heterostructures," *arXiv preprint arXiv:1403.4985*, 2014.

[8] X. Hong, J. Kim, S.-F. Shi, Y. Zhang, C. Jin, Y. Sun, S. Tongay, J. Wu, Y. Zhang, and F. Wang, "Ultrafast charge transfer in atomically thin mos2/ws2 heterostructures," *Nature nanotechnology*, 2014.

[9] M. Li, D. Esseni, G. Snider, D. Jena, and H. G. Xing, "Single particle transport in two-dimensional heterojunction interlayer tunneling field effect transistor," *Journal of Applied Physics*, vol. 115, no. 7, p. 074508, 2014.

[10] D. Esseni, P. Palestri, and L. Selmi, *Nanoscale MOS transistors: Semi-classical transport and applications*. Cambridge University Press, 2011.

[11] J. Bardeen, "Tunnelling from a many-particle point of view," *Phys. Rev. Letters*, vol. 6, 1961.

[12] R. M. Feenstra, D. Jena, and G. Gu, "Single-particle tunneling in doped graphene-insulator-graphene junctions," *Journal of Applied Physics*, vol. 111, no. 4, pp. 043 711–043 711, 2012.

[13] L. Britnell, R. Gorbachev, A. Geim, L. Ponomarenko, A. Mishchenko, M. Greenaway, T. Fromhold, K. Novoselov, and L. Eaves, "Resonant tunnelling and negative differential conductance in graphene transistors," *Nature communications*, vol. 4, p. 1794, 2013.

[14] R. Schlaf, C. Pettenkofer, and W. Jaegermann, "Band lineup of a sns2/snse2/sns2 semiconductor quantum well structure prepared by van der waals epitaxy," *Journal of applied physics*, vol. 85, no. 9, pp. 6550–6556, 1999.

[15] R. Schlaf, O. Lang, C. Pettenkofer, and W. Jaegermann, "Band lineup of layered semiconductor heterointerfaces prepared by van der waals epitaxy: Charge transfer correction term for the electron affinity rule," *Journal of applied physics*, vol. 85, no. 5, pp. 2732–2753, 1999.

[16] L. Upadhyayula, J. Loferski, A. Wold, W. Giriat, and R. Kershaw, "Semiconducting properties of single crystals of n-and p-type tungsten diselenide (wse2)," *Journal of Applied Physics*, vol. 39, no. 10, pp. 4736–4740, 1968.

[17] G. Domingo, R. Itoga, and C. Kannewurf, "Fundamental optical absorption in sn s 2 and sn se 2," *Physical Review*, vol. 143, no. 2, p. 536, 1966.

[18] D. Abdel Hady, H. Soliman, A. El-Shazly, and M. Mahmoud, "Electrical properties of $snse_2$ thin films," *Vacuum*, vol. 52, no. 4, pp. 375–381, 1999.

[19] J. S. Ross, P. Klement, A. M. Jones, N. J. Ghimire, J. Yan, D. Mandrus, T. Taniguchi, K. Watanabe, K. Kitamura, W. Yao *et al.*, "Electrically tunable excitonic light-emitting diodes based on monolayer wse2 pn junctions," *Nature nanotechnology*, vol. 9, no. 4, pp. 268–272, 2014.

[20] C. Sergio, Q. Gao, and R. M. Feenstra, "Theory of graphene–insulator–graphene tunnel junctions," *Journal of Vacuum Science & Technology B*, vol. 32, no. 4, p. 04E101, 2014.

[21] K. T. Lam, G. Seol, and J. Guo, "Operating principles of vertical transistors based on monolayer two-dimensional semiconductor hetero-junctions," *Applied Physics Letters*, vol. 105, no. 1, p. 013112, 2014.

[22] L. De Michielis, L. Lattanzio, and A.-M. Ionescu, "Understanding the superlinear onset of tunnel-fet output characteristic," *Electron Device Letters, IEEE*, vol. 33, no. 11, pp. 1523–1525, 2012.

[23] B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C.-Y. Yang, C. Tabery, C. Ho, Q. Xiang, T.-J. King, J. Bokor, C. Hu, M.-R. Lin, and D. Kyser, "Finfet scaling to 10 nm gate length," in *Electron Devices Meeting, 2002. IEDM '02. International*, Dec 2002, pp. 251–254.

[24] Y. Chauhan, D. Lu, S. Venugopalan, M. Karim, A. Niknejad, and C. Hu, "Compact models for sub-22 nm mosfets," in *Proc. Workshop Compact Model*, 2011.

[25] A. M. van der Zande, J. Kunstmann, A. Chernikov, D. A. Chenet, Y. You, X. Zhang, P. Y. Huang, T. C. Berkelbach, L. Wang, F. Zhang *et al.*, "Tailoring the electronic structure in bilayer molybdenum disulfide via interlayer twist," *Nano letters*, vol. 14, no. 7, pp. 3869–3875, 2014.

[26] S. Datta, F. Assad, and M. S. Lundstrom, "The silicon mosfet from a transmission viewpoint," *Superlattices and Microstructures*, vol. 23, no. 3, pp. 771–780, 1998.

[27] K. Bernstein, R. Cavin, W. Porod, A. Seabaugh, and J. Welser, "Device and architecture outlook for beyond cmos switches," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2169–2184, Dec 2010.

[28] D. Nikonov and I. Young, "Uniform methodology for benchmarking beyond-cmos logic devices," in *Electron Devices Meeting (IEDM), 2012 IEEE International*, Dec 2012, pp. 25.4.1–25.4.4.

[29] ——, "Overview of beyond-cmos devices and a uniform methodology for their benchmarking," *Proceedings of the IEEE*, vol. 101, no. 12, pp. 2498–2533, Dec 2013.

[30] C.-H. Lee, G.-H. Lee, A. M. van der Zande, W. Chen, Y. Li, M. Han, X. Cui, G. Arefe, C. Nuckolls, T. F. Heinz *et al.*, "Atomically thin pn junctions with van der waals heterointerfaces," *arXiv preprint arXiv:1403.3062*, 2014.

[31] S. Vishwanath, X. Liu, S. Rouvimov, J. K. Furdyna, D. Jena, and H. G. Xing, "Molecular beam epitaxy of layered material superlattices and heterostructures," *Bulletin of the American Physical Society*, 2014.

[32] L. Cheng, X. Qin, A. T. Lucero, A. Azcatl, J. Huang, R. M. Wallace, K. Cho, and J. Kim, "Atomic layer deposition of a high-k dielectric on mos2 using trimethylaluminum and ozone," *ACS applied materials & interfaces*, vol. 6, no. 15, pp. 11 834–11 838, 2014.

[33] T. Roy, M. Tosun, J. S. Kang, A. B. Sachid, S. Desai, M. Hettick, C. C. Hu, and A. Javey, "Field-effect transistors built from all two-dimensional material components," *ACS nano*, 2014.

[34] H. Fang, S. Chuang, T. C. Chang, K. Takei, T. Takahashi, and A. Javey, "High-performance single layered wse2 p-fets with chemically doped contacts," *Nano letters*, vol. 12, no. 7, pp. 3788–3792, 2012.

[35] L. Yang, K. Majumdar, Y. Du, H. Liu, H. Wu, M. Hatzistergos, P. Hung, R. Tieckelmann, W. Tsai, C. Hobbs *et al.*, "High-performance mos 2 field-effect transistors enabled by chloride doping: Record low contact resistance (0.5 k$\omega\cdot$ μm) and record high drain current (460 μa/μm)," in *VLSI Technology (VLSI-Technology): Digest of Technical Papers, 2014 Symposium on*. IEEE, 2014, pp. 1–2.

[36] H. Xu, E. Kinder, S. Fathipour, A. Seabaugh, and S. Fullerton-Shirey, "Reconfigurable ion doping in 2h-mote2 field-effect transistors using peo:csclo4 electrolyte." The 41st International Symposium on Compound Semiconductor, May 2014.
[37] R. Kappera, D. Voiry, S. E. Yalcin, B. Branch, G. Gupta, A. D. Mohite, and M. Chhowalla, "Phase-engineered low-resistance contacts for ultrathin mos2 transistors," *Nature materials*, 2014.